What are MOSPOWER® FETs?

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Vertical Metal-Oxide-Semiconductor Field-Effect Transistors uniquely combine the advantages of the power bipolar transistor with those of the MOSFET. The result is a high-power, high-voltage, high-gain power transistor with no minority-carrier storage time, no thermal runaway and a greatly inhibited secondary breakdown characteristic, all of which are contributing to the spectacular rise in the popularity of the MOSPOWER FET.

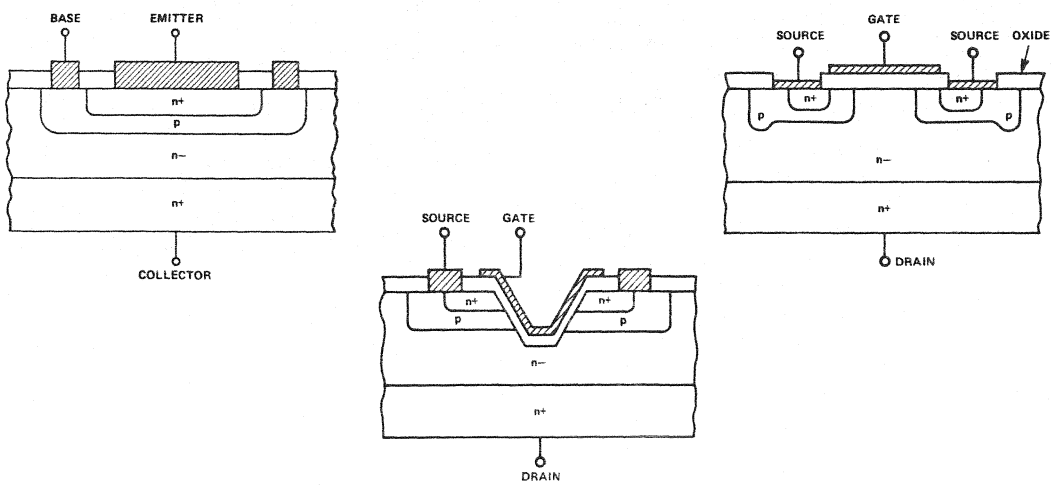
Construction of the MOSPOWER FET

Within the MOSPOWER FET family there are two basic topologies: a low-voltage V-groove structure, commonly called VMOS, and a high-voltage double-diffused planar structure called DMOS. In their initial stage of fabrication both closely resemble the double-diffused epitaxial power transistor with an n^+ substrate followed by an n^- epitaxial into which is first diffused a p and then an n^+ layer forming a 4-layer structure.

One distinguishing feature of VMOS, as shown in Figure 1, is the anistropically-etched V-groove cut normal to the surface that extends through both the n^+, p and penetrates slightly the n^- epitaxial region. By virtue of this V-groove easy access is provided for the gate to overlay the p-diffusion which acts as the current conducting channel.

DMOS resembles planar topology even though the drain current path penetrates through the n^- epitaxy and the n^+ substrate to the backside contact. The current path through the p diffusion channel is established exactly as it is for the VMOS structure. A positive gate potential (for an n-channel MOSPOWER FET) inverts the p-channel and the resulting electron-enhanced n-channel, extending from the n^+ source to the n^- epi, offers an uninterrupted, low resistance current path devoid of the thermal properties associated with the typical bipolar transistor.

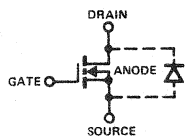
Another distinguishing feature is the electrical bonding of the uppermost n^+ diffusion (source) to the p diffusion (body). In the bipolar model this would tie the base to the emitter; for the MOS model it ties the source to the body. Without this electrical bond there would exist a parasitic 4-layer npn bipolar in parallel with the MOSPOWER FET thus masking the beneficial features with the problems encountered with bipolar transistors. However, with this electrical bond, a source-drain parasitic diode appears in parallel with the MOSPOWER FET.



A Comparison of a 4-Layer Bipolar Transistor with VMOS & DMOS
Figure 1

The "Beneficial" Parasite — The Body-Drain Diode

All power MOSFETs, irrespective of topology (or tradename) have a body-drain *pn* junction that appears in shunt with the channel as shown schematically in Fig. 2. Fortunately, by virtue of the polarity of this parasitic diode, performance is virtually unaffected under normal operation. This parasitic is of mixed blessing; on the one hand, a parasitic element is undesirable from an aesthetic viewpoint, but practically speaking, a reverse polarity diode intrinsic to the FET structure becomes a useful snubbing diode when the power FETs are arranged in a totem-pole configuration such as in motor control applications. If, however, the power FETs are to be used as low resistance analog switch gates then care must be taken to arrange their polarity to achieve high OFF isolation, as shown in Fig. 3. For detailed application information the reader is encouraged to review Application Note AN77-2 "Don't Trade Off Analog Switch Specs."



Schematic Representation of VMOS Showing Body-Drain Diode
Figure 2

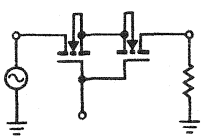


Figure 3

The vertical MOS structure, like the power bipolar transistor, offers a large surface area for source metal and the entire backside of the chip for the drain. This is of great importance as it allows maximum current carrying capacity unavailable to a nonvertical structure.

Early in the history of power MOSFETs some indecision existed relative to the need of static gate protection and for a short time lower power MOSFETs were found with zener gate protection. Although highly recommended for small-signal MOSFETs, power MOSFETs with substantial gate-to-source capacity do not need alternative means for static protection.

The absence of the zener offers considerable freedom. Where before, with the zener-protected gate, the user was cautioned never to allow the gate polarity to reverse (swing negative for an *n*-channel MOSFET), now without the zener the gate is free to swing as far as its breakdown rating in either polarity.

Controlling the MOSPOWER Transistor

Operationally, MOS is unique among power transistors. Channel conduction is proportional to gate *voltage, not* to any sort of injection current, typical of the bipolar transistor. Whatever input current that does exist beyond that attributed to leakage may be identified as the charging current necessary to overcome the input capacitance in very high-speed switching situations. Because the steady-state gate current is negligible, the familiar parameter, *Beta*, is of little importance. Consequently, MOS exhibits a high input resistance that makes it ideal for many logic control applications.

Gate-Source Breakdown

Some confusion exists with respect to the maximum allowable gate-to-source voltage a power MOSFET can safely handle. *It is seldom equal to the absolute maximum drain-gate voltage.*

Several operating parameters of the power FET—among them the gate control voltage—depend upon the oxide thickness that separates the gate from the bulk semiconductor: the MOSFET structure itself. To achieve control with reasonable voltages the gate to source voltage—predicated by the oxide thickness—is limited to ±30V.

This means that if the power FET is perched atop a high-voltage rail, such as the uppermost device in a totem-pole configuration, you must be careful to keep the gate voltage within the safe limits with respect to the *source of the same FET.* This same precaution also applies for some source-follower applications and for many gating applications especially when the source is riding on a rail voltage in excess of 30V.

There are a variety of procedures for driving a power MOSFET sitting high above the safe operating voltage limits and the reader is encouraged to review Application Notes AN79-4, "Driving the MOSPOWER FET," AN80-1, "MOSPOWER FETs—A Key to the Advancement of SMPS Technology."

MOS as a Switch: Turning it ON

Driving MOS from logic requires an appreciation of the gate drive power needed to actuate, or turn *on*, the MOS power transistor. First, the driver must be able to deliver sufficient current during the transition (from *off* to *on*) to adequately charge the input capacitor in the desired time. Two familiar equations show that to achieve a high speed switch driving the gate from a low impedance, high current source is certainly desirable.

$$t = 2.2\ R_g \cdot C_{in}$$

$$i = C_{in}\ dV/dT$$

where R_g = input resistance
C_{in} = input capacity
dV/dT = rate of voltage change

As this driving voltage ramps upward another phenomenon occurs called *Miller effect*. Once the threshold voltage of the MOS transistor is passed it begins to draw increasingly heavier drain current. In Figure 4 the rapid use of drain current with respect to the gate voltage is clearly illustrated. As the drain current rises, the transconductance rises rapidly to saturation as shown in Figure 5. Concurrent with this rise in transconductance is a proportional rise in gain and the once low feedback capacitance now swells to enormous proportions appearing as an addition to the input capacitance.

$$C_{in} = C_{iss} + (1 + A_V)C_{gd}$$

where C_{iss} = common-source input capacitance
C_{gd} = gate-drain capacity
A_V = voltage gain

If the driver is deficient in its reserve of drive current the MOS transistor's switching speed suffers and the waveform shown in Figure 6 is the inevitable result. On the other hand, if the driver can deliver the required charging current the switching speed is determined solely by just how fast the driver *can* deliver.

Turning the Switch OFF

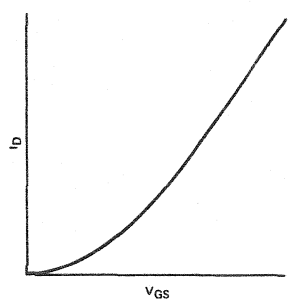
Turn off is another story where the MOS power transistor outperforms its equivalently-rated power bipolar transistor. MOS, a majority-carrier transistor begins to turn off immediately upon the removal of gate voltage. Again the speed is limited by the rate of discharge of the input capacitor through the driver. For ultra-high speed switching special charge transfer circuits are recommended for dumping current both into and out of the MOS gate. Upon the removal of the gate voltage the MOSPOWER FET 'shuts down' (a fail-safe feature?), the resistance between drain and source rises to a very high value and whatever current flow that remains is limited to leakage. This, of course, precludes that the breakdown voltage is not reached.

The Characteristics of MOS

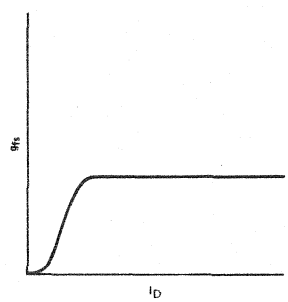
Closer examination of Figure 1 reveals that MOS, unlike the conventional low power MOSFET, has a very short channel where, as the drain-source current flow increases, electron velocity saturation results. The consequences resulting from this velocity saturation are three-fold: the output characteristics assume a constant-current plateau, the forward transconductance saturates and, most important, a linear transfer characteristic results. All of these effects are shown collectively in Figures 4, 5 and 7.

The Importance of Threshold Voltage

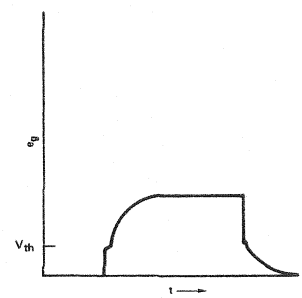
As an enhancement-mode MOSFET, we see what appears as a delayed turn-on when a voltage ramp is applied to the gate. This apparent delay is, in reality, caused by the threshold voltage level, below which the channel remains nonconducting and above which drain current begins. A logic-compatible MOS is one whose threshold voltage is set so that in the low state [0] the MOS is *off* and in the high state [1] the MOS is *on*. It is important to note that a low threshold voltage is undesirable for high power MOS devices for a number of reasons. High power MOS transistors generally operate at higher chip temperatures for optimum efficiency. Since threshold is temperature dependent (a coefficient of approximately -5 mV/°C) a high threshold is mandated to assure operation in the enhancement region. Furthermore, high-power devices have large input capacitance which necessitates a substantial drive. The wisdom of a high threshold precludes the possibility of driver noise causing false triggering of the MOS. This noise immunity is especially important when working in switching power supplies and motor control applications.



Transfer Characteristics of VMOS Showing Linear I_D/V_{GS} Relationship
Figure 4



Transconductance vs Drain Current
Figure 5



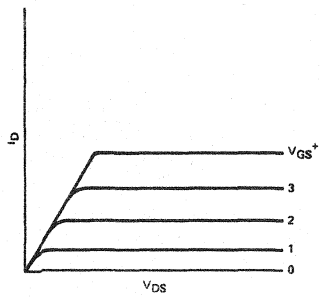
Effect in Input Waveform When Miller Effect Loads Driver Excessively
Figure 6

Temperature Effects of MOS

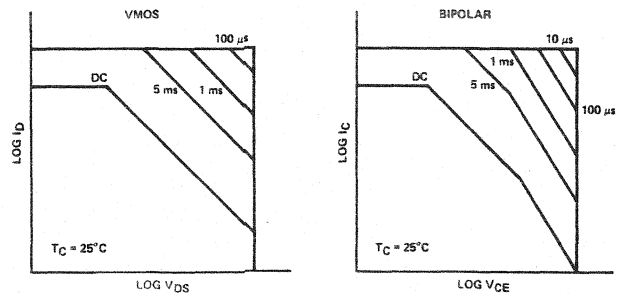
The negative temperature coefficient of gain characteristic of FETs is certainly a valuable asset when using MOS in linear applications, for it greatly simplifies the biasing circuitry. As a bulk semiconductor the resistance of the silicon exhibits a positive temperature coefficient of 0.6%/°C.

The benefits from this unique thermal property are twofold. MOS offers an exceptionally stable SOA *(safe operating area)* in comparison to equivalently-rated power bipolar transistors as shown in Figure 8. Secondly, paralleling MOS for increased current handling presents no problem. Any intrinsic unbalance between MOS transistors does not result in current hogging because the negative temperature characteristic acts to equalize the current flow.

Always be careful to keep MOS power transistors within their operating temperature limits. If heat sinks are advisable, use them.



Output Characteristics of VMOS
Figure 7



Typical Safe Operating Area
Comparison Between MOS and Bipolar
Figure 8